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Radiation-Hardened Silicon-on-Insulator 0.8-μm Technology Design Rules

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ADMINISTRATIVE INFORMATION

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INTRODUCTION

Compared to the junction isolation of very large scale integration (VLSI) technologies based on bulk silicon, the full dielectric isolation afforded by silicon on insulator (SOI) offers many well-known advantages. Of primary importance is the significant reduction in parasitic junction capacitance that results from replacing the silicon under the source/drain regions with an insulator. This reduction in capacitance yields higher device switching speed and decreased dynamic power consumption. Additional SOI benefits include reduced interconnect capacitance, unconditional latch-up immunity, insensitivity to transient radiation and single-event phenomena, and the process simplicity inherent to the natural device isolation. Due to full dielectric isolation, the source, drain, p-well, and n-well design rules become limited only by the alignment capability of the lithographic tool and the ability to transfer patterns by dry-etching. These advantages lead to processing simplicity and very high density circuitry.

An SOI technology has been developed at SSC San Diego for radiation-hardened applications. This technology is based on a 0.8-micron minimum feature size and is designed to be a highly reliable, manufacturable process. Although primarily developed for radiation-hardened military applications, this SOI process can be used to great effect in commercial and non-radiation-hardened military applications. The presence of the insulating layer, together with the bulk silicon handle wafer, provides many applications to MEMs technology. The lowered parasitic capacitance affords the possibility of RF systems on a chip. Similarly, SOI technology makes low-voltage and low-power circuitry possible without sacrificing speed. Because of the reduced junction area and leakage, SOI technology is also suited for high-temperature environments. All these characteristics can be combined to create smart sensors and other demanding applications in this technology.

This document gives specifications on the layout design rules and simulation program with integrated circuit emphasis (SPICE) models to construct and simulate complementary metal oxide semiconductor (CMOS) circuits designed in the SOI technology developed at the Integrated Circuit Research & Fabrication Branch at SSC San Diego.

0.8-MICRON DOUBLE-LEVEL METAL RADIATION-HARDENED SILICON-ON-INSULATOR (RHSOI) CMOS DESIGN RULES

The SSC San Diego RHSOI process is in development. SSC San Diego is investigating a mesa-isolated, double-level-metal, salicide process in addition to a shallow-trench isolation process. The cornerstone of the process is the use of 200-nm-thick films of specially developed separation by implantation of oxygen (SIMOX). The buried oxide is 380 nm. The process includes incorporation of a lightly doped drain (LDD) for reduction of electric fields and, hence, reduced radiation sensitivity. SSC San Diego is developing two type of body contacts: (1) body tied to source (BTS), where the source of the transistor is connected to the channel by an opposite polarity source/drain implant; and (2) body node contact (BNC), where silicon is brought out from underneath the poly gate and contacted separately from the source/drains. Preliminary design rules have been developed for these two types of body ties. Variations on design rules are left to the discretion of the experiment's designer, as the

photolithography, alignment, and pattern transfer are reasonable for SSC San Diego's tool set. A second layer of metal is based on a resist-planarized and etched-back, low-temperature oxidate (LTO) film for interlevel dielectric.

The photolithography is based on a GCA XLS I-Line 4X stepper using positive resist for all layers. The process uses plasma reactive ion etching (RIE) for the silicon islands, Poly, Contact, Via, Metal1, and Metal2 layers. Table 1 lists the GDSII layer numbers and descriptions that should be used for this technology. Table 2 describes and details the SSC San Diego RHSOI CMOS process flow.

Table 1. GDSII layer names and numbers.

Layer Name	Alias	Synonym	GDSII Layer Number:
Island	ISL	Active	1
Pminus	PM	Pwell	2
Nminus	NM	Nwell	3
Poly	POL	Gate	4
Pplus	PPL		5
Nplus	NPL		6
TiN	TIN		7 (not currently supported)
Contact	CON		8
Metal1	M1	Met1	9
Via1	VIA1		10
Metal2	M2	Met2	11
Passivation	PAS	Pad, Overglass	12
Nedge	NE	Edge	14 (optional)
Capacitor	CAP		19 (for linear capacitors, optional)
Resistor	RES		20 (silicide blanking layer)
Via2	VIA2		21
Metal3	M3	Met3	22

Table 2. SSC San Diego RHSOI CMOS process flow.

Description	Details
Starting SOI thickness	200-nm SIMOX
Island isolation	Plasma etch
NMOS threshold implant	
PMOS threshold implant	
Gate oxidation	Tox = 15 nm
Polysilicon deposition,doping, etch	TPOLY= 380 nm
NMOS LDD implant	
PMOS LDD implant	
Sidewall oxide deposition	300-nm undoped LTO
Sidewall oxide etch	plasma etch
NMOS source/drain implant	
PMOS source/drain implant	
Source/drain anneal	
Titainium deposition	T = 50 nm
Silicon implant	
RTA	
Ti etch	
RTA	
Contact oxide, etch contacts	300-nm undoped LTO
Metal deposition, etch	500-nm: TiW/ Al 1%Si Ti
Sinter	
1st LTO	500 nm
Planarizing Resist, etchback	
2nd LTO	550 nm
Metal deposition, etch	750 nm: Ti/ Al/1% Si / Ti
Sinter	
Passivation	900-nm PSG, 300-nm LTO cap.

The minimum drawn gate length is 0.8 μm with a nominal effective gate length of 0.8 μm. No biasing of any masks are performed before mask fabrication. Gate oxide thickness is 14 to16 nm, final poly thickness is 380 nm, final spacer oxide width is 200 nm, contact oxide is 300-nm LTO under metal1. Metal1 is a stack of TiW/ Al 1%Si Ti. Both Contact and Via holes are etched with a wet/dry process to create "champagne glass" profiles. Metal2 is a stack of Ti/ Al/1% Si / Ti to improve step coverage and reduce hillock formation. The targeted parameters for intermetal dielectric and Metal2 are 550-nm planarized LTO and 7500 A, respectively. Phospho silicate glass (PSG) is used at the passivation step to provide for gettering, although PSG may be used for the contact oxide. There is no BPSG/reflow capability at this time.

Table 3 lists three of the most important transistor parameters: mobility (U0), threshold voltage (VTO), and gate oxide thickness (TOX) for NMOS and PMOS devices in this technology. Table 4 lists what can be expected out of the process for contact and sheet resistances. Table 5 summarizes the design rules for a 1.2-μm technology for comparison. If density is not required, yield can be improved by using the design rules in the last column of table 5. Table 6 summarizes the process and device parameters for the RHSOI 0.8-μm process. The parameters that are not filled in are either not applicable for SOI technology, or no statistical data are presently available.

Table 3. NMOS and PMOS target device parameters.

Target Device	NMOS	PMOS
U0	500	200
VTO	0.80	–0.91
TOX	150	150

Table 4. Typical process parameters.

Process	Parameter
Contact resistance	0.5 to 2.0 ohms
Island sheet resistance	2 to 4 ohms/square
Poly sheet resistance	2 to 4 ohms/square

Table 5. Design rules summary.

RULE	1.2 um Minimum Rules	0.8 um Minimum Rules	Recommended If Density Not Required
SILICON ISLAND			
Width	1.2	1.2	1.2
Separation	1.2	1.2	1.2
Overlap p+ or n+	1.2	0.6	1.2***
Minimum source/drain width	2.4	1.8	2.4
POLY			
Width	1.0	0.8	0.8
Spacing	1.4	1.0	1.4
Extension past ISLAND	1.0	0.8	1.0
Field POLY to ISLAND spacing	1.2	1.0	1.2
CONTACT			
Minimum CONTACT opening	1.2	1.0	1.2
Minimum CONTACT spacing	1.8	1.2	1.8
Minimum separation between CONTACT and POLY gate.	1.8	1.0	1.8
Minimum overlap of POLY around CONTACT	1.2	0.6	1.2
Minimum overlap of ISLAND around CONTACT	1.2	0.6	1.2
METAL 1			
Minimum METAL1 width	1.6	0.8	2.0
Minimum METAL1-METAL1 spacing	1.4	1.2	2.0
Minimum METAL1 overlap of CONTACT	1.2	0.6	1.2
VIA1			
Minimum VIA opening	1.8 x 1.8	1.2 x 1.2	2.0 x 2.0
Minimum overlap of METAL1 around VIA	1.2	0.6	1.2
Minimum VIA-to-CONTACT separation	1.8	1.2	1.8
Minimum VIA-to-VIA spacing	1.8	1.2	1.8
METAL 2			
Minimum METAL2 width	2.0	1.2	2.0
Minimum METAL2-METAL2 spacing	1.8	1.6	2.0
Minimum METAL2 overlap of VIA	1.2	0.6	1.2

***NOTE: BODY TIE RULE IS 0.6um

Table 6. Process and device parameters for SSC San Diego RHSOI 0.8-µm process.

Device Parameter	Units	N-Channel	P-Channel
Threshold voltage	Volts	0.7 to 0.9	-0.9 to -1.0
K prime (uCox/2	A/V^2	*	
Delta L (total)	microns	0.0 to 0.1	0.0 to 0.1
Delta W (total)	microns	0.0 to 0.1	0.0 to 0.1
Bulk threshold	(Volts)^1/2	*	
Oxide thickness	Angstroms	140 to 160	140 to 160
Lateral diffusion (per side)	microns	< 0.2	<0.2
Junction capacitance	pF/cm^2	*	
Junction sidewall capacitance	pF/cm	*	
Gate overlap capacitance	pF/cm	*	
Diffusion sheet rho	Ohms/square	< 5	<5
Poly sheet rho	Ohms/square	< 5	<5
Field threshold	Volts	*	
P-well sheet rho	Ohms/square	*	
N-well sheet rho	Ohms/square	*	
Metal 2 sheet rho	Ohms/square	< 0.1	
Metal 1 sheet rho	Ohms/square	<0.2	
Metal 2 to Metal 1 capacitance	pF/cm2	*	
Metal2 to poly capacitance	pF/cm2	*	
Metal1 to poly capacitance	pF/cm2	< 10*10**3	
Metal2 to field capacitance	pF/cm2	*	
Metal1 to field capacitance	pF/cm2	*	
Poly to field capacitance	pF/cm2	*	
Metal2 to AA capacitance	pF/cm2	*	
Metal1 to AA capacitance	pF/cm2	*	
Metal2 to metal1 resistance	Ohms	< 0.5	
Metal1 to poly resistance	Ohms	<10	
Metal1 to AA resistance	Ohms	< 10	
Punch-through	Volts	*	
Junction breakdown voltage	Volts	*	
Subthreshold slope	mV/Dec	<100	<120
Channel leakage	pA/micron	<10	<1.0
Operating voltage range	Volts	3.0 to 5.5	

NOTE:

*Parameter to be determined.

GENERAL PROCESS SPECIFICATIONS

The following tables describe general process specifications. Table 7 lists dielectric thickness specifications. Table 8 lists transistor specifications. Sheet resistance specifications are listed in table 9. Table 10 lists contact and via resistance specifications. Table 11 lists parasitic capacitance value specifications and table 12 lists maximum current specifications. Where no values are listed, it is left to the user to fill in measured values.

Table 7. Dielectric thickness.

Parameter	Specification
Gate oxide	150 +/–15 A
Field oxide	3000 +/–500 A
Buried oxide	3800 +/–200 A
Metal1 to PolySi oxide	3000 +/–500 A
Metal2 to Metal2 (over poly on fox)	5500 +/–500 A
Metal2 to Metal1 (over fox near topography)	7850 +/–500 A
Metal2 to Metal1 (over fox no topography)	5500 +/–500 A

Table 8. Transistor specifications.

Parameter	Specification
P-channel transistor (10 μ/10 μ)	
Threshold voltage	–0.9 ± –0.1 V
K' = uCox	38 μA/v^2
Ids with Vds = –5v, Vgs = –5v (10 x 0.8)	1.7 mA
Subthreshold slope (10 x 0.8)	95 mV/Decade
N-channel transistor (10 μ/10 μ)	
Threshold voltage	0.8 ±0.1 V
K' = μCox	96 μA/v^2
Ids with Vds = –5v, Vgs = –5v (10 x 0.8)	2.7 mA
Subthreshold slope (10 x 0.8)	110 mV/Decade

NOTE: The K' values only apply to low source drain voltages where the transistor is not in saturation. (T = 25ºC).

Table 9. Sheet resistances (ohms per square).

Parameter	Specification
P±Island	3 ±1.0 ohms
N±Island	3 ±0.7 ohms
Un-implanted Island	3 ±0.7 ohms
P±Poly	3 ±1.0 ohms
N±Poly	3 ±1.0 ohms
Un-implanted Poly	3 ±1.0 ohms
Metal1	150.0 ±50 milliohms/square
Metal2	60.0 ±10 milliohms/square

NOTE: Silicide process, 200-nm silicon island thickness.

Table 10. Contact and via resistance (1.2 u x 1.2 u drawn contact or via).

Parameter	Specification (ohms)
Metal-1 to Metal-2 V	0 .2 ±0.1
P-island to Metal-1 Contact	1.0 ±0.2
N-island to Metal-1 Contact	1.0 ±0.2
Poly-Si to Metal-1 Contact	1.1 ±0.3

Table 11. Parasitic capacitance values.

Parameter	Specification
Gate oxide plate	2.30 ±0.10 fF/um^2

Table 12. Maximum current specification.

Parameter	Specification
Maximum current through 1.2 x 1.2 drawn contact to active	
Static	____mamps
Peak	____mamps
Maximum current through 1.2 x 1.2 drawn via	
Static	____mamps
Peak	____mamps

SPICE LEVEL 3 MODELS

As was stated in the introduction, for this partially depleted technology, there are two structures of SOI transistors. They differ significantly in their layout and performance and, hence, SPICE models are developed to account for these differences. Figures 1 and 2 show the H-gate and BTS device structure with some of the parasitic elements schematically overlaid. Tables 13 and 14 are the SPICE level 3 models. Generic SPICE was developed for bulk Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs). To model an SOI device requires some modifying assumptions.

The parameter that is used for source and drain resistance is RSH (sheet resistance in ohms/square). To get the proper RSD for each transistor, set NRS, NRD (the # of squares) = 1/W (i.e. RSH = 500, W = 10 μm, NRS = NRD = 0.1, RSD = 50. CGDO and CGSO have been adjusted to match measured ring oscillator speeds. CGDO and CGSO are multiplied by PD and PS respectively, the Source drain perimeter, which in the case of BTS devices is equal to *Wdrawn* or for H-gate devices is equal to *Wdrawn+* lengths of the "H." Notice CJ has been set to the buried oxide capacitance, and MJ has been set to a low value to simulate a linear capacitor to the substrate. CJ is multiplied by AS and AD , the areas of the source and drain regions, to get the absolute capacitance. (See figures 1 and 2 to see how AD and AS are defined). Notice also that CGBO is used for H-gates, and considers the legs of the H-gate that overlap the channel region. CGBO is set to zero for BTS devices although there is a non zero amount of overlap capacitance from the poly-on-field to substrate. Because of this, BTS devices are generally faster than H-gate devices. CJSW is used for the capacitance of source/drain to channel. This is because CJSW is F/m and is multiplied by PS and PD, the perimeter of the source and drain regions, which in the case of BTS devices, is equal to *Wdrawn,* or for H-gate devices, is equal to *Wdrawn+* lengths of the "H." For SOI, there is very little source/drain to channel/substrate area and, hence, very little capacitance. XJ = junction depth = silicon film thickness = 0.2 μm.

Body resistance and placement of body ties become important for transistor operating limits, high-frequency operations, operations where charge storage is critical, and radiation sensitivity—especially transient effects. Body ties need to be spaced close together for reduction of floating body effects (FBE) such as the "kink" in saturation, "snapback," and early breakdown. Note that figures 1, 2, and 3, body ties for BTS devices decrease the effective width, and H-gates are limited to a design rule width before needing placement in parallel for higher current needs.

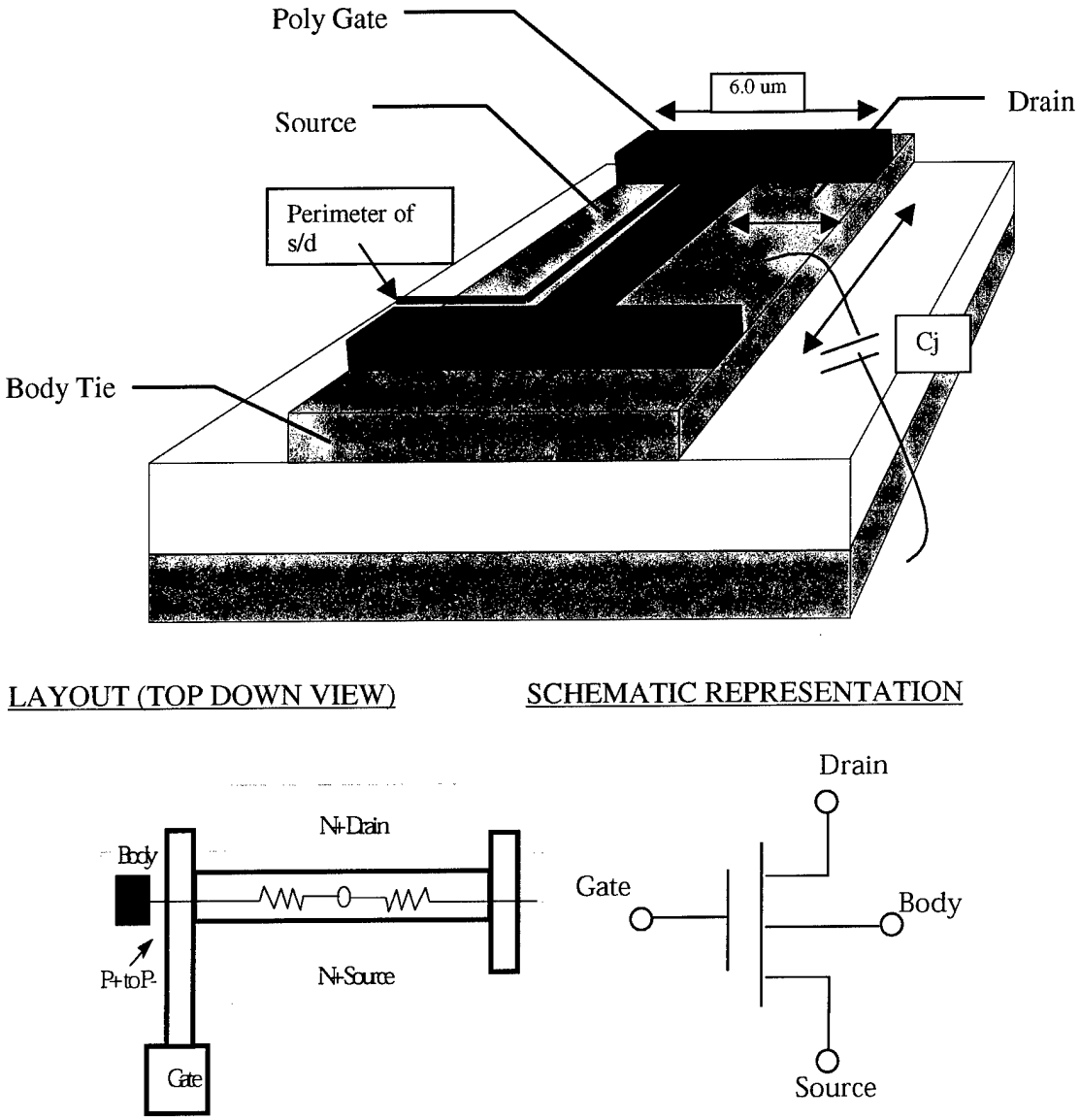

Figure 1. H-gate SOI structure. Physical structure, layout, and schematic representations of H-gate silicon-on-insulator device.

Table 13. Level 3 SPICE parameters for H-gate NMOS and PMOS.

```
* THESE LEVEL 3 MODELS ARE BASED ON SPAWAR SOI LOT 1866 WAFER 1713-76
* USE THE FOLLOWING EQUATIONS TO CALCULATE AD, AS, PD, PS, NRD, NRS:
* AD=AS=(W METERS)*(2.6E-6 METERS)
* PD=PS=(W METERS)+(5.2E-6 METERS)
* NRD=NRS=(1E6/(W METERS))
* EXAMPLE: W=10U=10E-6METERS --> AD=AS=(10E-6*2.6E-6)=26E-12
*               --> PD=PS=(10E-6+5.2E-6)=15.2E-6
*                              --> NRD=NRS=(1E6/10E-6)=0.1
* CJ is multiplied by AD and AS. MJ is artificially set low to approximate a linear
capacitor.
* CJSW is calculated from extracted NSUB and Silicon film thickness, and is multiplied by PD
and * PS.
* CGBO for H-gate is calculated from the dimension of the legs of the "H" (5.2um)and the
gate
* oxide thickness, and is multiplied by L.
* CGDO, and CGSO are fitted to ring oscillator speeds.
*
* MODEL NHG5XP8 MODEL EXTRACTED FROM DEVCICE WITH W=5U L=0.8U
.MODEL NHG5XP8 NMOS (   LEVEL=3          VTO    = 0.9842533
+TOX    = 1.55E-8     UO    = 520       THETA  = 0.0273409
+LD     = 6.229969E-8  WD    = -4.945256E-7  RSH    = 804
+NSUB   = 2.006847E17  GAMMA  = 1.1585489   ETA    = 5E-3
+KAPPA  = 0.05       VMAX   = 1.127127E5   XJ     = 2E-7
+NFS    = 2E11       DELTA  = 5.9585902   PHI    = 0.8505747
+PB     = 0.62       CGBO   = 2.8E-8
+CJSW   = 3.280E-10   CGDO   = 2.0E-10     CGSO   = 2.0E-10
+CJ     = 8.62E-5     MJ     = .01        MJSW   = 0.5)

* MODEL NHG10X10 EXTRACTED FROM DEVICE WITH W=10U L=10U
.MODEL NHG10X10 NMOS ( LEVEL=3          VTO    = 0.965
+TOX    = 1.55E-8     UO    = 401.6802333  THETA  = 0.0178887
+LD     = 6.229969E-8  WD    = -4.945E-7   RSH    = 804
+NSUB   = 2.006847E17  GAMMA  = 1.1585489   ETA    = 5E-3
+KAPPA  = 0.05       VMAX   = 1.127E5     XJ     = 2E-7
+NFS    = 2E11       DELTA  = 1E-3        PHI    = 0.8505747
+PB     = 0.62       CGBO   = 2.8E-9      CJSW   = 3.280E-10
+CGDO   = 2.0E-10     CGSO   = 2.0E-10
+CJ     = 8.62E-5     MJ     = .01        MJSW   = 0.5)
```

```
* MODEL PHG5XP8 EXTRACTED FROM DEVICE WITH W=5U L=0.8U
.MODEL PHG5XP8 PMOS (   LEVEL=3          VTO    = -0.8524494
+TOX    = 1.55E-8     UO    = 231.8104071   THETA  = 0.2144133
+LD     = 9.19687E-8    WD    = -4.928749E-7  RSH    = 1.32E3
+NSUB   = 6.995093E16   GAMMA  = 0.6839967    ETA    = 5E-3
+KAPPA  = 1.3        VMAX  = 1.237853E5    XJ     = 2E-7
+NFS    = 3E11       DELTA  = 0.4961303    PHI    = 0.796056
+PB     = 0.62       CGBO  = 2.8E-8      CJSW   = 1.936E-10
+CGDO   = 2.0E-10     CGSO  = 2.0E-10
+CJ     = 8.62E-5     MJ    = .01       MJSW   = 0.5)

* MODEL PHG10X10 EXTRACTED FROM DEVICE WITH W=10U L=10U
.MODEL PHG10X10 PMOS (  LEVEL=3          VTO    = -0.918
+TOX    = 1.55E-8     UO    = 174.8533632   THETA  = 0.14
+LD     = 9.19687E-8    WD    = -5.424497E-7  RSH    = 1.32E3
+NSUB   = 6.995093E16   GAMMA  = 0.6839967    ETA    = 5E-3
+KAPPA  = 1.3        VMAX  = 1.237853E5    XJ     = 2E-7
+NFS    = 3E11       DELTA  = 1E-3       PHI    = 0.796056
+PB     = 0.62       CGBO  = 2.8E-9      CJSW   = 1.936E-10
+CGDO   = 2.0E-10     CGSO  = 2.0E-10
+CJ     = 8.62E-5     MJ    = .01       MJSW   = 0.5)
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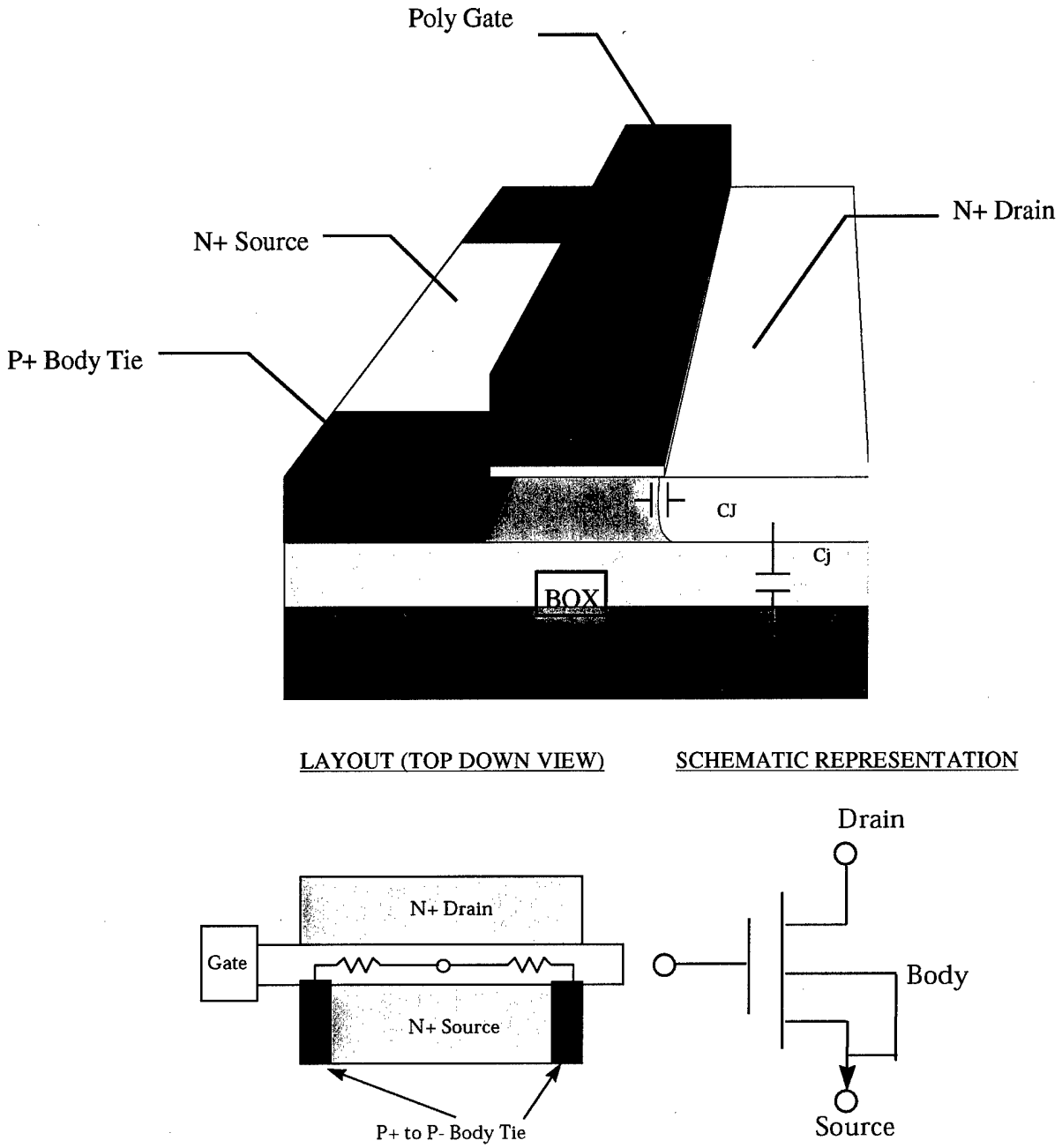

Figure 2. Body tied to source (BTS) SOI structure. Physical structure, layout and schematic representations of BTS silicon-on-insulator device.

Table 14. Level 3 SPICE parameters for BTS-gate NMOS and PMOS.

```
* THESE LEVEL 3 MODELS ARE BASED ON SPAWAR SOI LOT 1742 WAFER 1742-26
* USE THE FOLLOWING EQUATIONS TO CALCULATE AD, AS, PD, PS, NRD, NRS:
* AD=AS=(W METERS)*(width of island METERS); (minimum contact on island =2.6E-6 METERS)
* PD=PS=(W METERS)
* NRD=NRS=(1E6/(W METERS))
* EXAMPLE: W=10U=10E-6METERS --> AD=AS=(10E-6*2.6E-6)=26E-12
*                --> PD=PS=W=10E-6
*                --> NRD=NRS=(1E6/10E-6)=0.1
* DATE: Oct 27/98
* LOT: 1742          WAF: 1599-26
* DIE: X10Y3          DEV: nbts10x10
* Temp= 27
.MODEL N10X10 NMOS (                TOX  = 1.55E-8
+ NSUB  = 1.960388E17   VTO  = 0.758042    DELTA = 1E-3
+ UO   = 450        ETA  = 0.07       THETA = 0.0417082
+ VMAX  = 1.2E5       KAPPA = 1         RD   = 64.179485
+ RS   = 64.179485    RSH  = 641        NFS  = 1E11
+ XJ   = 2E-7       LD   = 4.393929E-8   WD   = 5E-7
+ PHI   = 0.850574    PB   = 0.62       CGBO  = 0
+ CJSW  = 3.280E-10   CGDO  = 2.0E-10    CGSO  = 2.0E-10
+ CJ   = 8.62E-5    MJ   = .01       MJSW  = 0.5)
*
* DATE: Oct 27/98
* LOT: 1742          WAF: 1599-26
* DIE: X7Y3          DEV: pbts10x10
* Temp= 27
.MODEL P10X10 PMOS (                TOX  = 1.55E-8
+ NSUB  = 4.7E16     GAMMA = 0.56      VTO  = -1.003
+ DELTA = 2.835147E-4   UO   = 180        ETA  = 0.01
+ THETA = 0.11       VMAX  = 2E5       KAPPA = 2.7
+ RD   = 149        RS   = 149        RSH  = 1.49E3
+ NFS  = 1.5E11      XJ   = 2E-7       LD   = -5E-9
+ WD   = 5E-7       PHI   = 0.850574    PB   = 0.62
+ CJSW  = 3.280E-10   CGDO  = 2.0E-10    CGSO  = 2.0E-10
+ CJ   = 8.62E-5    MJ   = .01       MJSW  = 0.5)
*
* DATE: Oct 27/98
* LOT: 1742          WAF: 1599-26
```

```
* DIE: X7Y3          DEV: nbts10x0.8
* Temp= 27
.MODEL N10X08 NMOS (                TOX  = 1.55E-8
+ NSUB  = 1.960388E17   VTO  = 0.95      DELTA = 1E-3
+ UO   = 450        ETA  = 0.02      THETA = 0.0418911
+ VMAX  = 1.4E5       KAPPA = 0.2        RD   = 66.2168398
+ RS   = 66.2168398   RSH  = 662        NFS  = 1E11
+ XJ   = 2E-7       LD   = 5.143677E-8   WD   = 5E-7
+ PHI   = 0.850574     PB   = 0.62       CGBO  = 0
+ CJSW  = 3.280E-10   CGDO  = 2.0E-10    CGSO  = 2.0E-10
+ CJ   = 8.62E-5     MJ   = .01       MJSW  = 0.5)
*
* DATE: Oct 27/98
* LOT: 1742          WAF: 1599-26
* DIE: X7Y3          DEV: pbts10x0.8
* Temp= 27
.MODEL P10X08 PMOS (                TOX  = 1.55E-8
+ NSUB  = 4.7E16      GAMMA = 0.56       VTO  = -0.85
+ DELTA = 2.835147E-4   UO   = 180        ETA  = 0.01
+ THETA = 0.11       VMAX  = 2E5        KAPPA = 2.7
+ RD   = 149        RS   = 149        RSH  = 1.49E3
+ NFS  = 1.5E11      XJ   = 2E-7       LD   = -5E-9
+ WD   = 5E-7       PHI   = 0.850574    PB   = 0.62
+ CJSW  = 3.280E-10   CGDO  = 2.0E-10    CGSO  = 2.0E-10
+ CJ   = 8.62E-5     MJ   = .01       MJSW  = 0.5)
*
.ENDL 1742_ 26
```

Notes on effective width, the lateral diffusion (width) SPICE model parameter. Figure 3 shows the possible current paths for both the H-gate and the BTS transistor structures. Note that current paths exist for the H-gate transistor that would tend to make the effective width larger than drawn for the BTS, the current paths are limited (crowded) due to the reverse-biased body tie diode, thereby reducing the effective width. From the following: **Weffective = Wdrawn-(WD)** it can be seen that for H-gates the WD is negative, and for BTS devices, WD is positive. This has an effect when trying to determine the mobility from linear transconductance curves.

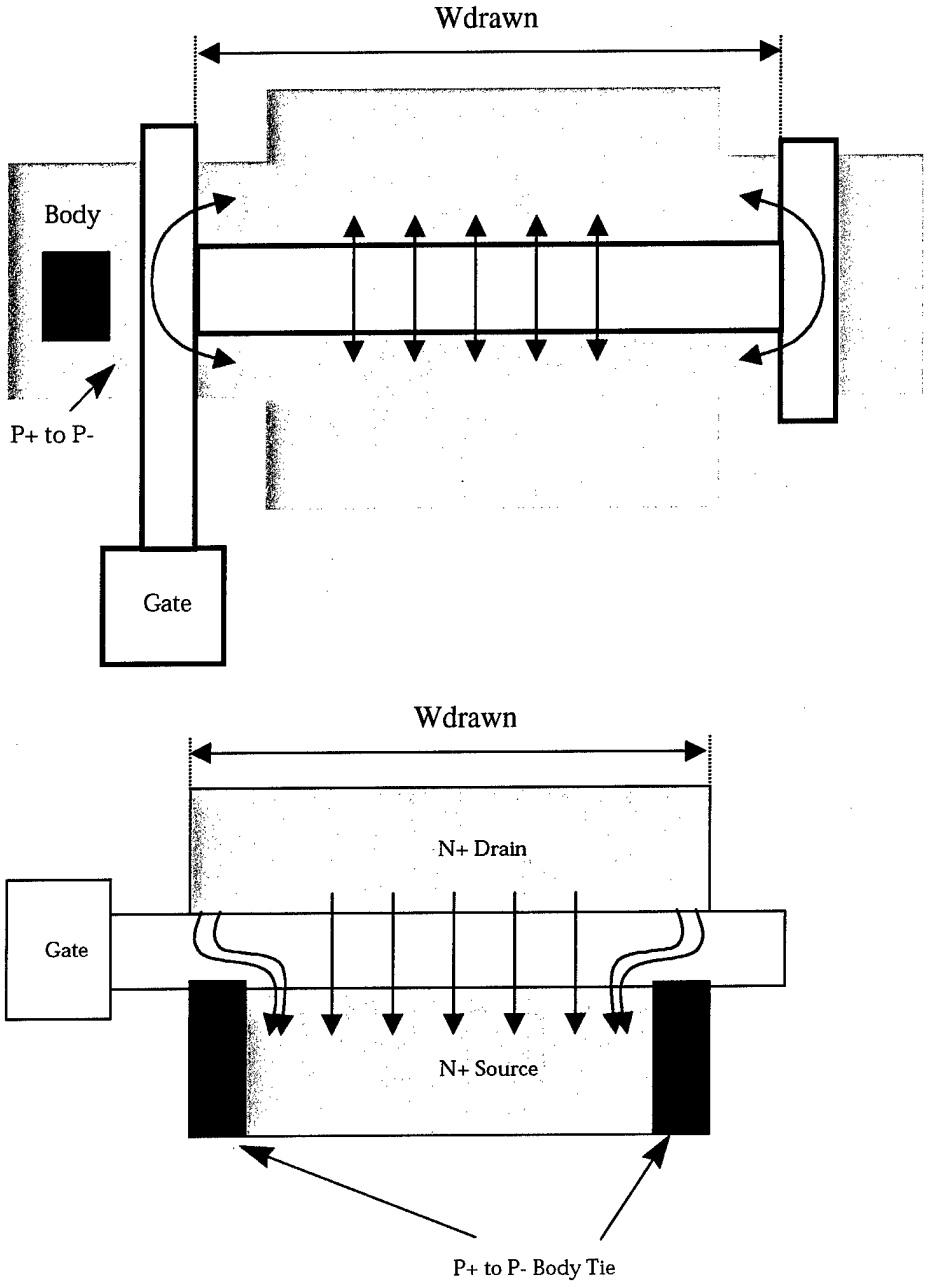

Figure 3. H-gate and BTS layout showing differences in effective width.

APPENDIX A
LAYOUT RULE NOTES

SSC San Diego targeted design rules are an outgrowth of CMOSN 1.0-μm rules, with a few modifications for compatibilty with future system requirements. Alternatively, CMOSN 1.2 μm or CMOSN 1.0-μm design rules may be used. Minimum rules should only be used when absolutely necessary. Smaller than minimum dimensions are allowable under certain circumstances (e.g., poly dimensions of 0.4 μm are possible with the I-line stepper). For more information on allowable design rules, contact Bruce Offord, D893, SSC San Diego. Table A-1 lists design layout rules. Figures A-1 through A-7 show the layout for each rule.

1. SILICON ISLAND

The rule for minimum silicon island (SI) width is 1.2 μm with 1.2-μm spacing. The thin (200-nm) silicon and total dielectric isolation allows for this tight spacing but should be investigated for leakage between islands under radiation.

2. NWELL, PWELL, N+, P+

The most important rule is the overlap of an implant around a silicon island. This rule is limited by the lithographic tool's alignment accuracy, which can be better than 0.4 μm but should be at least 1.0 μm for higher reliability. An exception to this rule is for a 0.6-μm overlap when there is a body contact involved. See figures A-11 and A-12 for example layouts of body ties.

3. POLY

The rule is 0.8/1.0 μm width/spacing and an overlap of silicon island of 0.8 μm. The present silicon etcher is an Applied 5000, with excellent pattern transfer so that the final poly width is almost exactly the drawn dimension of 1.0 μm. The minimum poly extension beyond island is 0.8 μm and the field poly spacing to island is 1.0 μm.

4. CONTACT (1.0/1.2 μm)

For lower resistance, use multiple contacts or larger than minimum contact size. The rules for enclosure of contact by island, poly, and Metal1 is 0.6 μm, which is within the stepper's alignment tolerance but for higher reliability should be at least 1.0 μm.

5. METAL1

The targeted rule is 0.8-/1.2-μm line/space. Variations on this rule need to be examined closely so that the resist planarization still meets the requirements.

6. VIA1

The rule 1.2/1.2 μm.

7. METAL2

The rule is 1.2/1.6 μm, although minimum rules should be avoided if it does not impact the density of design.

Table A-1. RHSOI 0.8-μm layout rules.

Figure #	Rule #	Rule	Minimum (μm)
A-1		Island	
	1A	Island width	
	1A1	Island width at FET	1.2
	1B	Island separation island	1.8
	1C	Implant overlap island	1.2
A-2		Polysilicon	
	2A	Polysilicon width	0.8
	2B	Polysilicon spacing in field	1.0
	2B1	Polysilicon separation to island	1.0
	2B2	Polysilicon spacing on island	1.0
	2C	Polysilicon overlap island	0.8
	2C1	Island overlap polysilicon (caps)	0.8
A-3		Contact	
	3A	Contact width	1.0
	3B	Contact separation	1.2
	3B2	Contact separation gate	1.0
	3C1	Island overlap contact	0.6
	3C2	Polysilicon overlap contact	0.6
A-4		Metal1	
	4A	Metal1 width	0.8
	4B	Metal1 spacing	1.2
	4C3	Metal1 overlap contact	0.6
A-5		Via	
	5A	Via width	1.2
	5B	Via spacing	1.2
	5B3	Via separation contact	1.2
	5C4	Metal1 overlap via	0.6
A-6		Metal2	
	6A	Metal2 width	1.2
	6B	Metal2 spacing	1.6
	6C5	Metal2 overlap via	0.6

Table A-1. RHSOI 0.8-μm layout rules. (Continued)

Figure #	Rule #	Rule	Minimum (μm)
A-7	7A	Implant overlap of poly gate	0.4
	7B	Implant overlap of Silicon at edge	0.6
	7B1	Implant width on Island	1.0
	7C	Implant extent from Poly	1.0
	7D	Metal2 separation of implants	1.0
	7D	Separation of implants	1.0
	7D	Separation of implants (MAXIMUM)	5.0

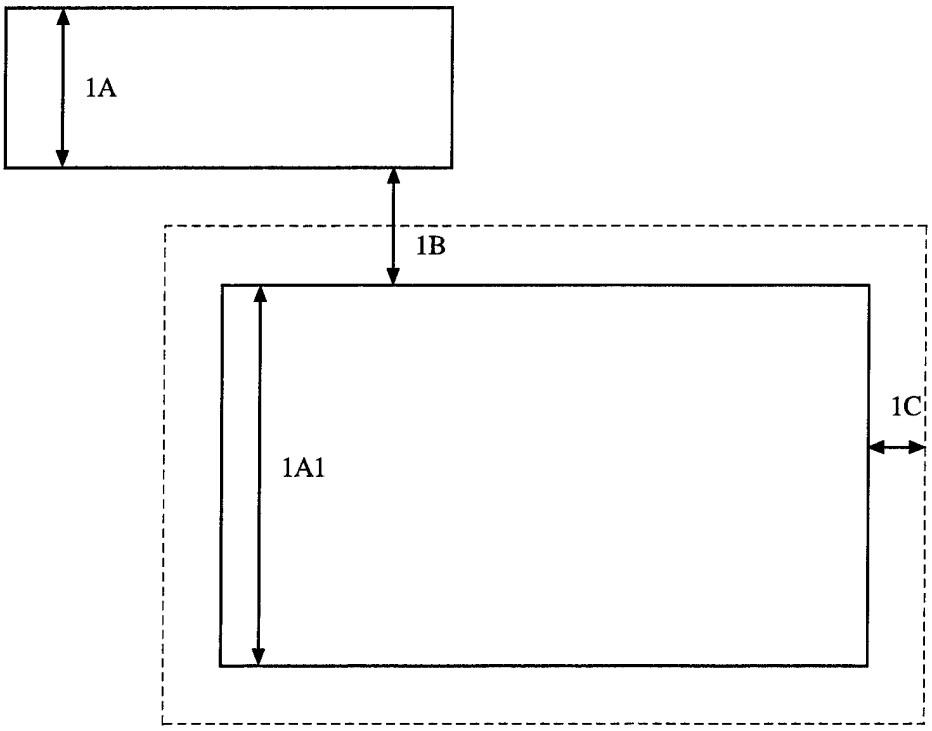

Figure A-1. Island rule.

Figure #	Island Rule #	Rule	Minimum (μm)
A-1	1A	Island width	1.2
	1A1	Island width at FET	1.8
	1B	Island separation Island	1.2
	1C	Implant overlap Island	0.6

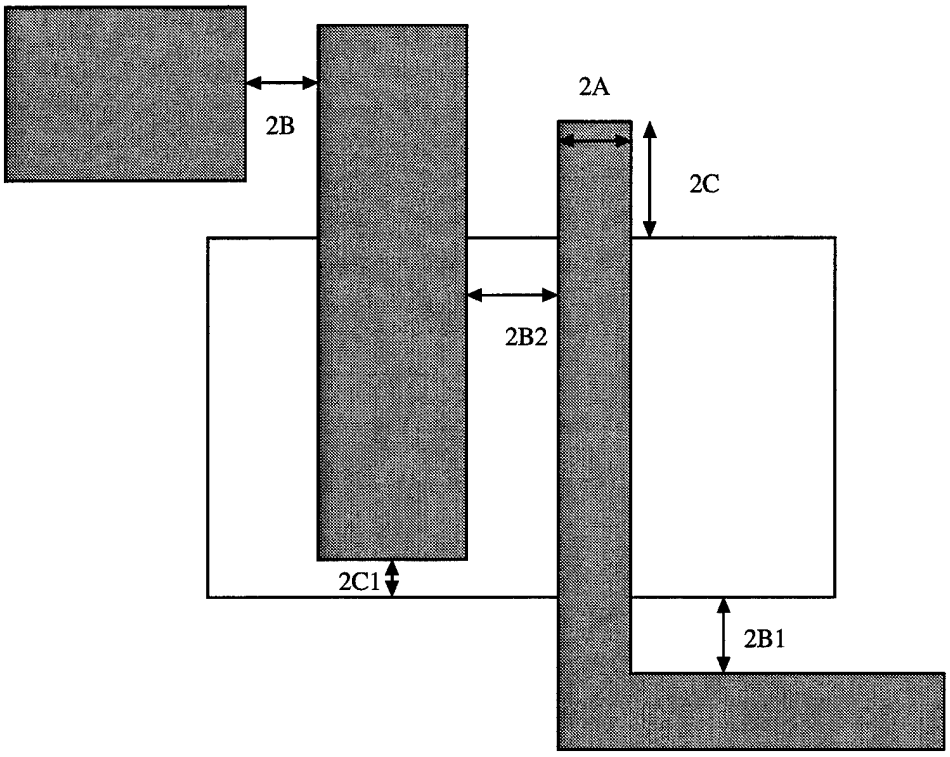

Figure A-2. Polysilicon rule.

Figure #	Polysilicon Rule #	Rule	Minimum (μm)
A-2	2A	Polysilicon width	0.8
	2B	Polysilicon spacing in field	1.0
	2B1	Polysilicon separation to island	1.0
	2B2	Polysilicon spacing on island	1.0
	2C	Polysilicon overlap island	0.8
	2C1	Island overlap polysilicon (caps)	0.8

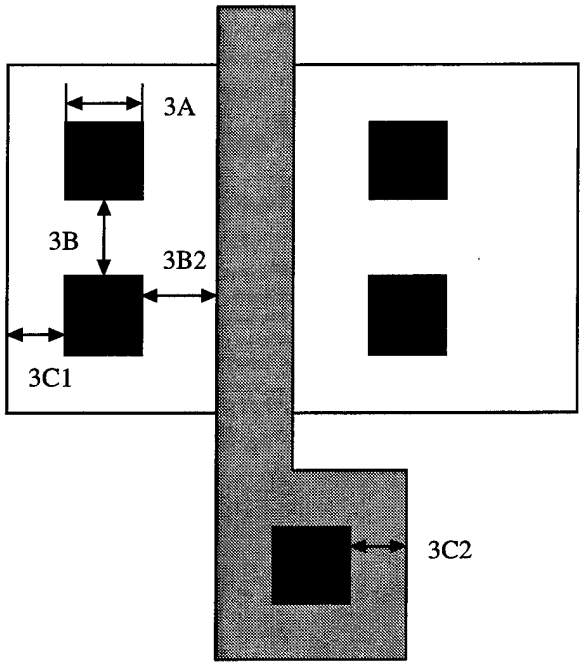

Figure A-3. Contact rule.

Figure #	Contact Rule #	Rule	Minimum (μm)
A-3	3A	Contact width	1.0
	3B	Contact separation	1.2
	3B2	Contact separation gate	1.0
	3C1	Island overlap contact	0.6
	3C2	Polysilicon overlap contact	0.6

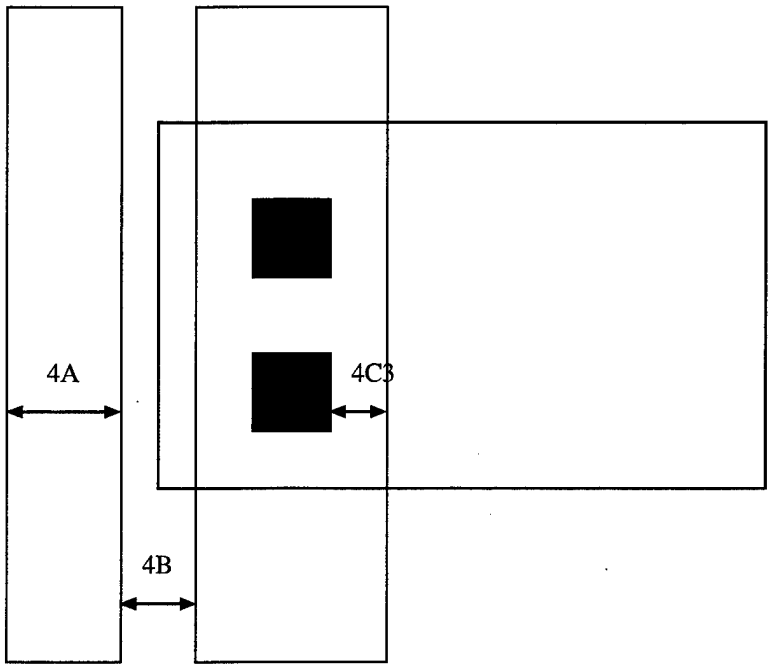

Figure A-4. Metal1 rule.

Metal1

Figure #	Rule #	Rule	Minimum (µm)
A-4	4A	Metal1 width	0.8
	4B	Metal1 spacing	1.2
	4C3	Metal1 overlap contact	0.6

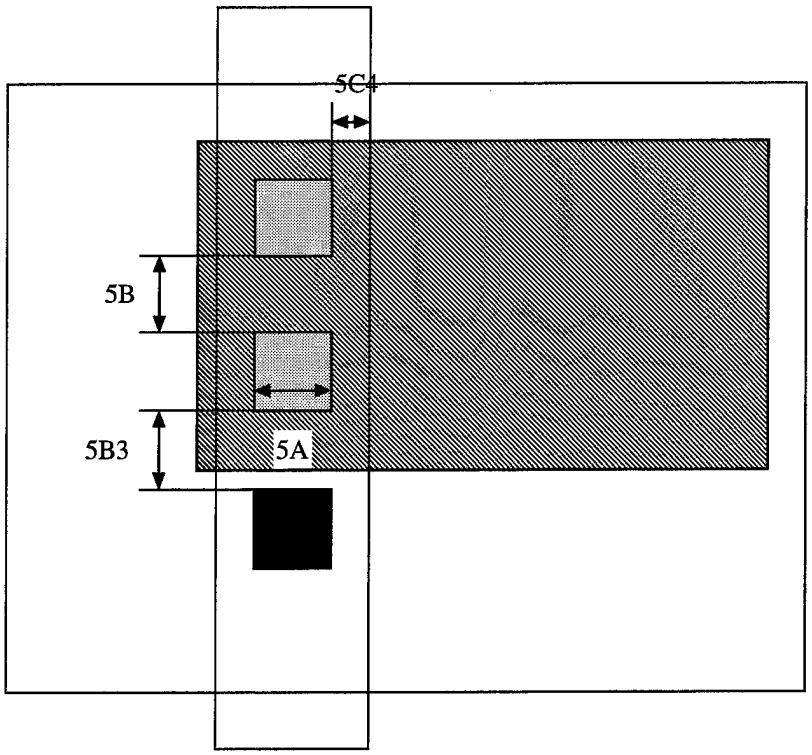

Figure A-5. Via rule.

Via1

Figure #	Rule #	Rule	Minimum (μm)
A-5	5A	Via width	1.2
	5B	Via spacing	1.2
	5B3	Via separation contact	1.2
	5C4	Metal1 overlap via	0.6

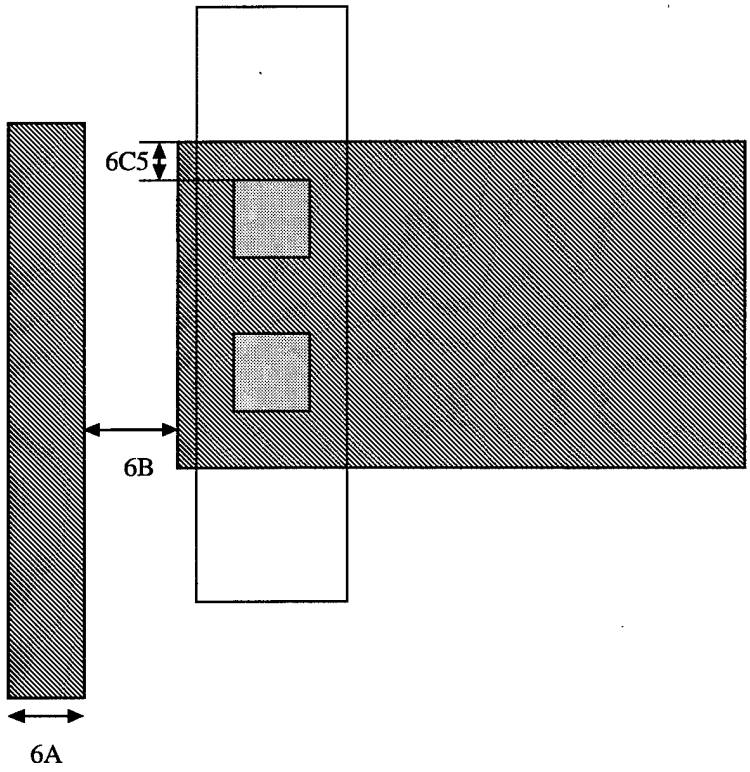

Figure A-6. Metal2 rule.

Figure #	Metal2 Rule #	Rule	Minimum (µm)
A-6	6A	Metal2 width	1.2
	6B	Metal2 spacing	1.6
	6C5	Metal2 overlap via	0.6

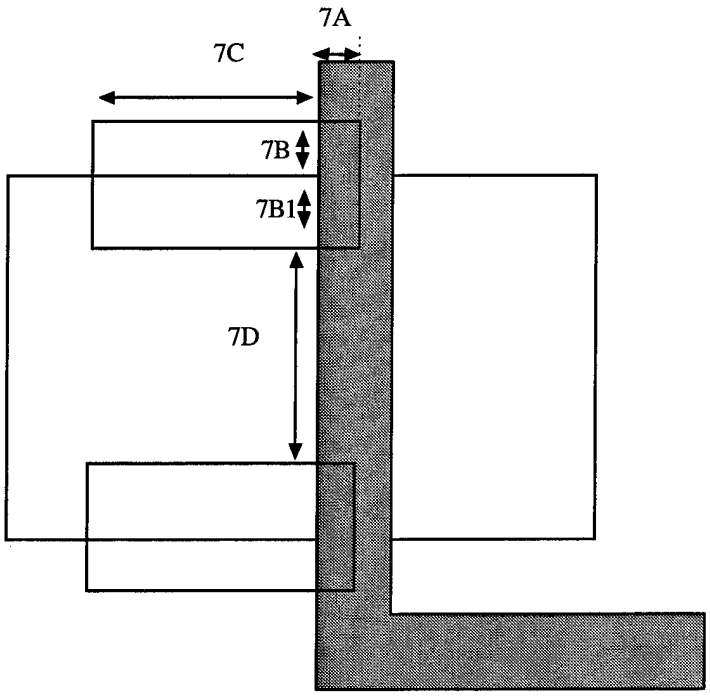

Figure A-7. Implant rule.

Figure #	BTS Rule #	Rule	Minimum (μm)
7	7A	Implant overlap of poly gate	0.4
	7B	Implant overlap of silicon at edge	0.6
	7B1	Implant width on island	1.0
	7C	Implant extent from poly	1.0
	7D	Separation of implants	1.0
	7D	Separation of implants (MAXIMUM)	5.0

Note: The source/drain implant is formed by the NOT of the BTS implant.

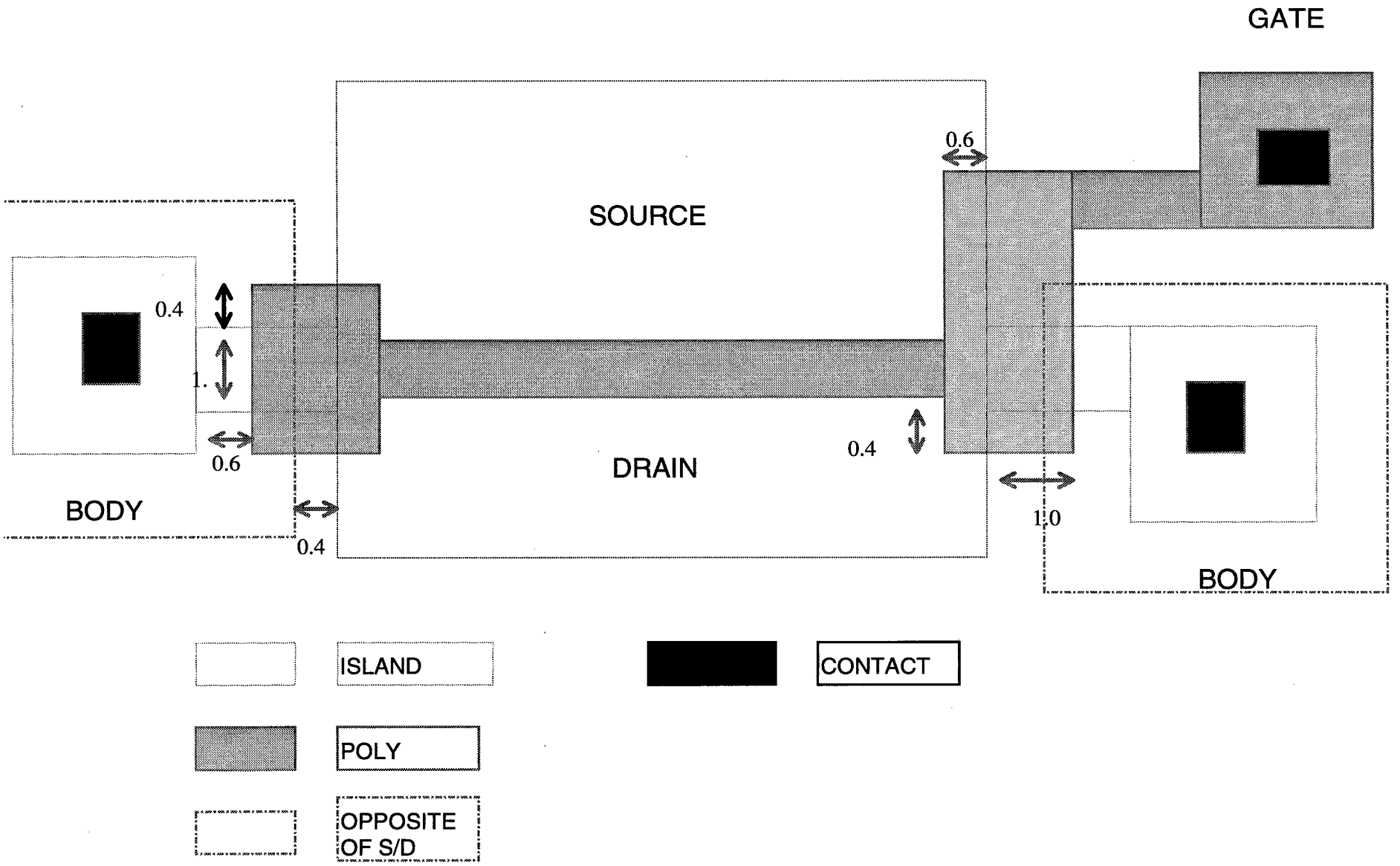

Figure 8. Example of double-body node contact.

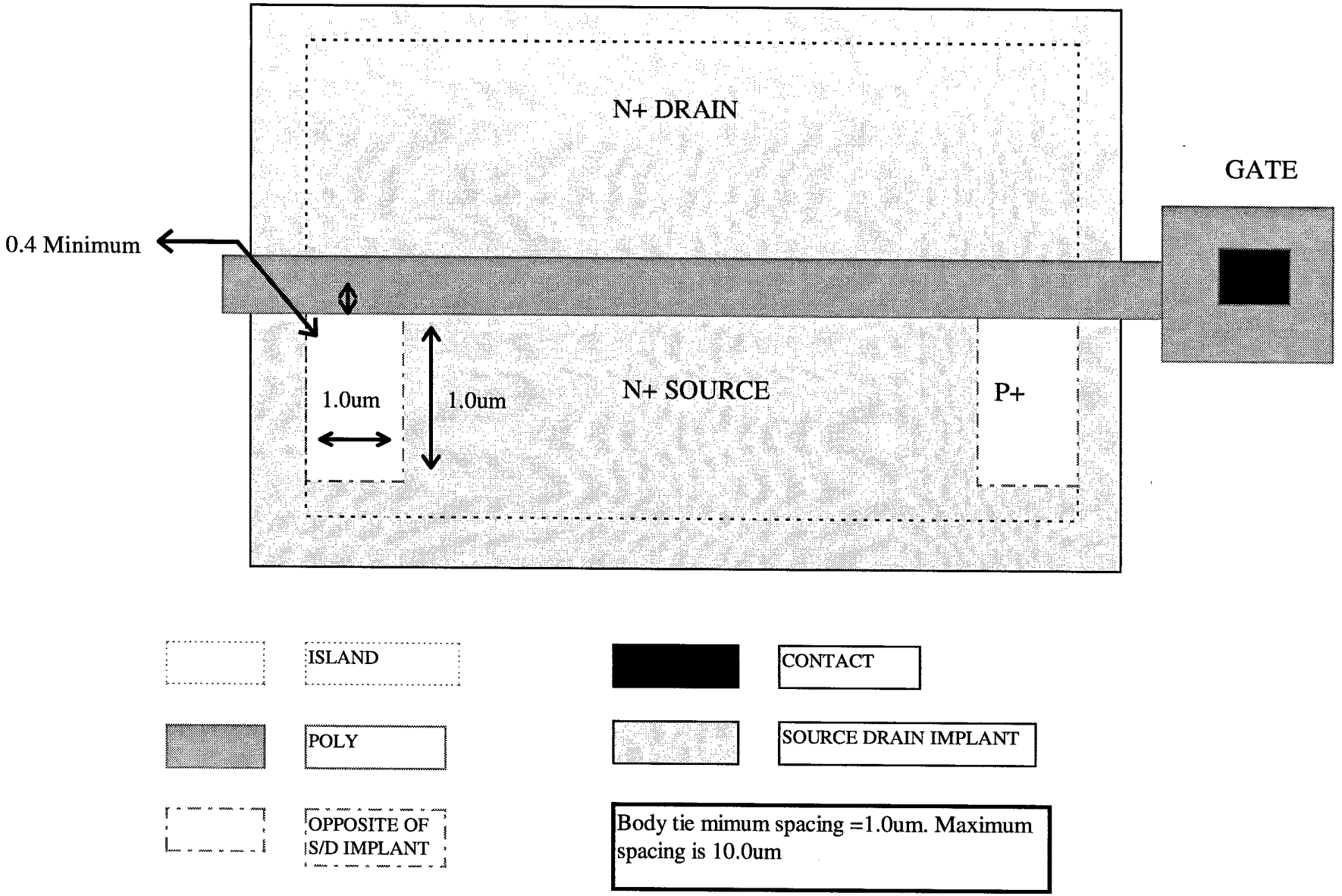

Figure-A-8. Example of body-tied to source contact.

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This document describes design rules for a radiation-hardened silicon-on-insulator (RHSOI) process presently under development at SSC San Diego. SSC San Diego's targeted design rules are an outgrowth of CMOSN 1.0-µm design rules, with a few modifications for compatibility with future system requirements. Alternatively, CMOSN 1.2-µm design rules may be used.

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